

SHAFT BOARD

USER MANUAL

1. INTRODUCTION

The SHAFT is a 6U, 1 slot VME board that is A24:D08:D16 compatible. The board accepts the LHC TTC and CTP signals, such as TURN, ORBIT, BC, and BUSY and, based on the logic implemented in FPGA, generates calibration triggers for three calibration systems of Tile detector. Calibration Request to the LTP (CTP) is also sent. The instances of the triggers are adjusted such as the calibration actions in the drawer will take place during so-called LHC Gap when no physics data is expected. One SHAFT board is designed to manage one out of four partitions of the Tile calorimeter. The trigger look-up table is loaded to RAM through VME bus allowing for flexible and easy change of the trigger sequences by users.

2. VME ADDRESSING

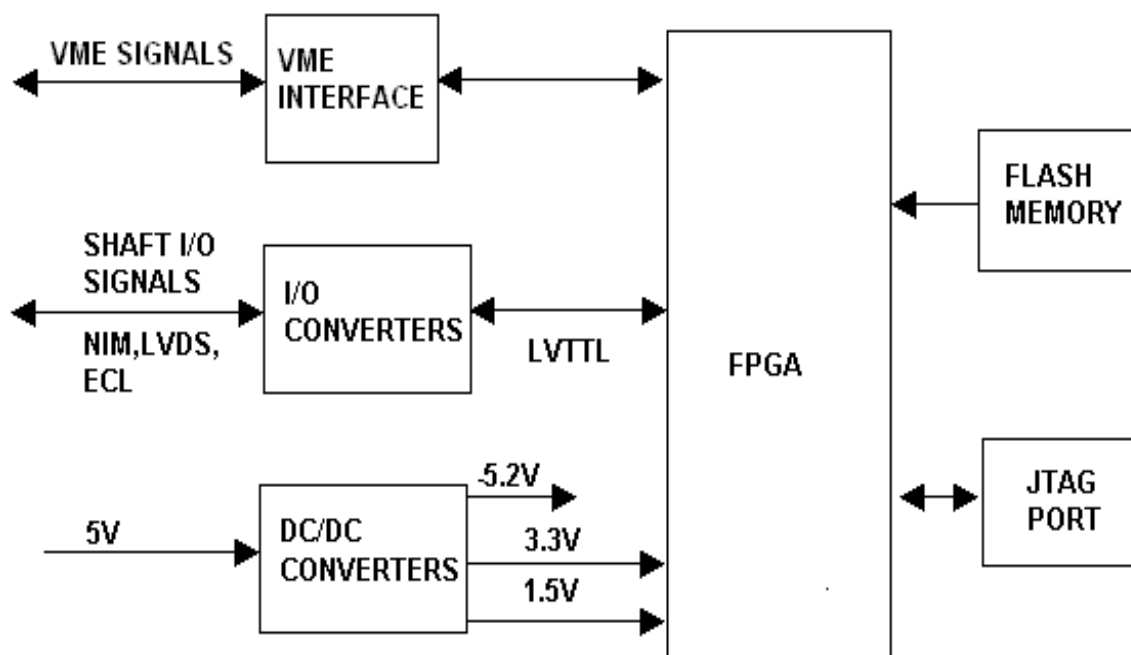
The VME address bus of the SHAFT board has 24 bits. The address is divided in two parts: BASE + OFFSET.

$$\text{BASE} = \text{VME_ADDRESS}(23..16)$$

$$\text{OFFSET} = \text{VME_ADDRESS}(15..0)$$

The base address is used to identify the SHAFT board in the VME crate, and the offset address is used to access to the internal RAM memory and registers of the board. The base address is set by configuring the two hexadecimal rotary switches of the board.

3. PARTS OF THE BOARD



The **FPGA** (Cyclone EP1C12Q240C6 from ALTERA) implements the VME protocol and the digital logic that is necessary to generate the calibration triggers.

The **FLASH memory** (EPC4QC100 from ALTERA) stores the program of the FPGA and loads this program to the FPGA each time the SHAFT board is powered on.

The **JTAG port** is useful to debug the code of the FPGA. Using a Byteblaster connector and the “SignalTapII logic analyzer” utility of the QUARTUSII software from ALTERA, the internal signals of the FPGA can be viewed on a PC screen. With the JTAG port the FPGA can be programmed directly (instead of programming the FLASH memory) eliminating necessity of power off and power on the board to update the code of the FPGA.

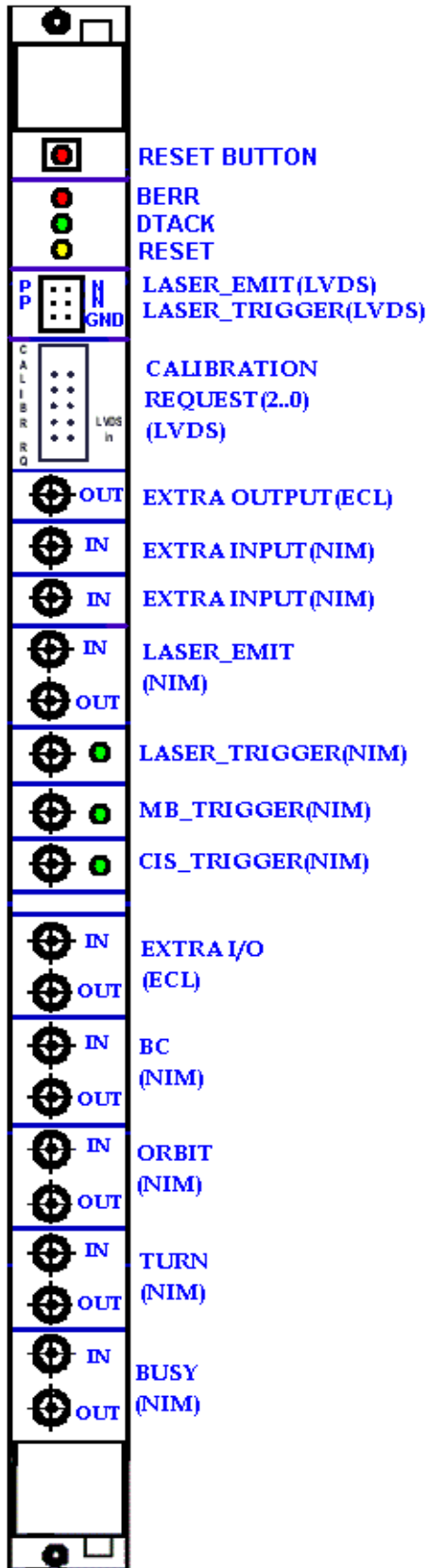
The **VME interface** is composed of input/output buffers that provide interface for the signals between the VME bus and the FPGA.

The **I/O converters** are the drivers and receivers that make conversion between the different I/O electrical standards: NIM, ECL, LVDS, and LVTTL (used in the I/O pins of the FPGA).

The SHAFT board hosts three **DC/DC converters**:

- **5V to -5.2V**: The -5.2V level is necessary to power the ECL and NIM I/O buffers.
- **5V to 3.3V**: The 3.3V level is used to power the FPGA and some LVTTL and CMOS buffers.
- **5V to 1.5V**: The 1.5V level is necessary to power the core of the FPGA.

4. FRONT PANEL AND I/O SIGNALS

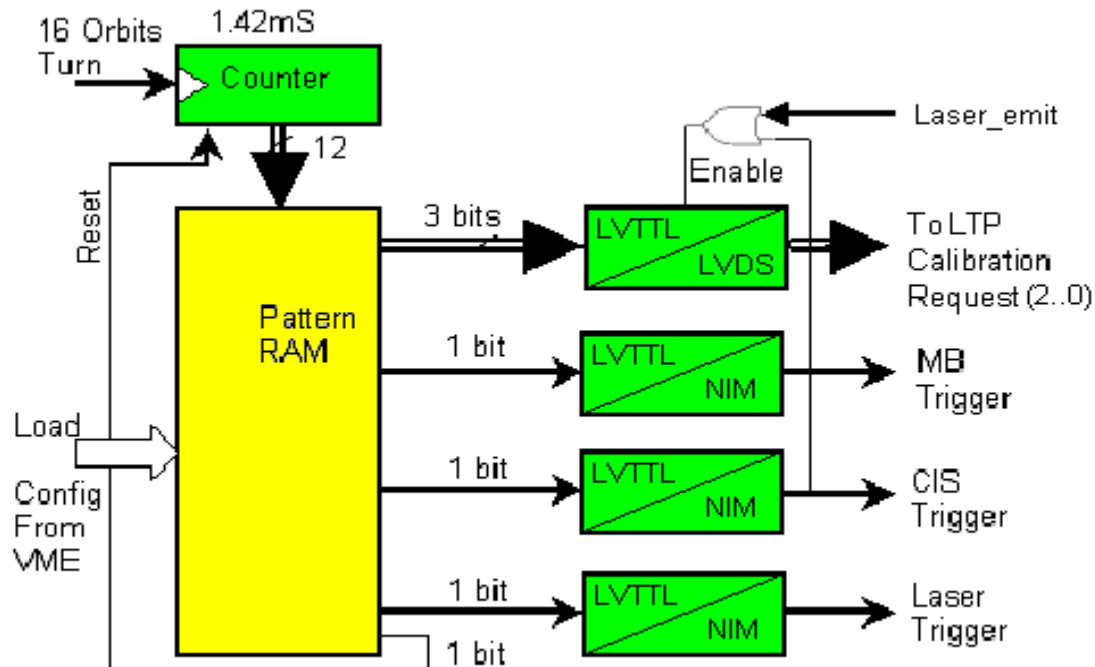


INPUTS	ELECTRICAL STANDARD
TURN (from LTP)	NIM
ORBIT (reserved)	NIM
BC (from LTP)	NIM
BUSY (from LTP)	NIM
LASER_EMIT (from SLAMA)	NIM
LASER_EMIT (from SLAMA)	LVDS
1 EXTRA INPUT (reserved)	ECL
2 EXTRA INPUTs (reserved)	NIM

OUTPUTS	ELECTRICAL STANDARD
TURN (monitoring)	NIM
ORBIT (monitoring)	NIM
BC (monitoring)	NIM
BUSY (monitoring)	NIM
LASER_EMIT (monitoring)	NIM
LASER_TRIGGER (to SLAMA)	NIM
LASER_TRIGGER (to SLAMA)	LVDS
CIS_TRIGGER (to TTCvi)	NIM
MB_TRIGGER (to TTCvi)	NIM
CALIBRATION_REQ(2..0) (to LTP)	LVDS
2 EXTRA OUTPUTs (not used)	ECL

Note: the inputs ORBIT, EXTRA input ECL, EXTRA input NIM and the EXTRA outputs ECL are reserved for if the functionality of the board has to be extended. They are not used in the current version of the board.

5. OPERATION



An accessible by the user part of the FPGA is pattern RAM (4 Kbytes) that is configured from the VME bus and is addressed by a 12 bits counter, driven by TURN input. Each position of the RAM has 8 bits: 3 bits for the calibration requests, 1 bit for the MB trigger, 1 bit for the CIS trigger, 1 bit for the Laser trigger, and 1 bit to reset the counter (the last bit is not used).

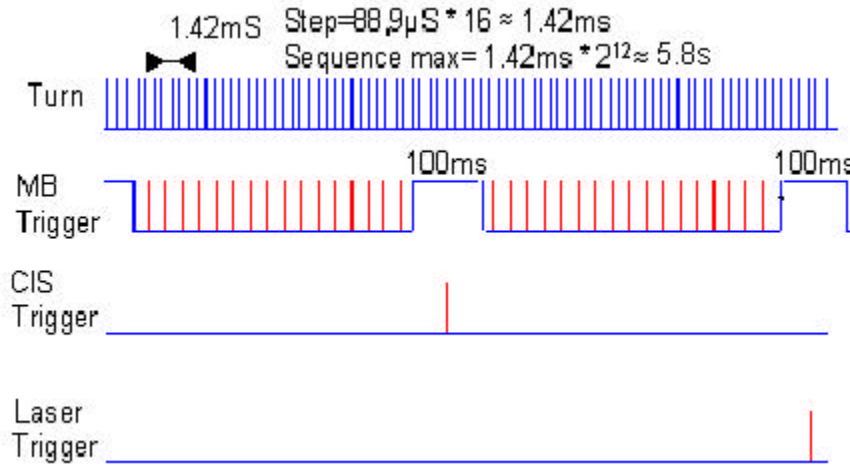
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not used	Reset counter	Laser trigger	CIS trigger	MB trigger	Cal_Req(2)	Cal_Req(1)	Cal_Req(0)

The 12 bits counter that addresses the pattern RAM is incremented by the TURN signal (from LTP). This signal arrives 1 time each 16 orbits (1.42 ms). If one of the trigger bits is set to '1' in some position of the RAM, the corresponding trigger is generated when the counter addresses that position. Only one of the three triggers (MB,CIS, LASER) should be set to '1' in the same memory position, otherwise none of the triggers will be generated. If the reset counter bit (bit 6) is set to '1' the TURN counter is reset .

The maximum trigger rate is defined by the frequency of the TURN input and is expected to be 1 trigger each 1.42 ms. The minimum trigger rate is 5.8s (4096*1.42 ms = 5.8s).

The MB triggers are suppressed for 50ms after and 50 ms before the Laser trigger or the CIS trigger is generated. The 50ms veto after the Laser and CIS triggers is implemented at the firmware level of the FPGA, but the 50ms veto before the Laser

and CIS triggers is controlled by the user while defining the pattern RAM. It is recommended to leave 35 positions of memory non-active after last MB trigger in a sequence of triggers and the next CIS or Laser trigger. The MB triggers are sent to a BGO input of the TTCvi.



The Laser triggers are sent to the SLAMA module. After this the SLAMA sends back to the SHAFT signal called Laser_emit. The calibration request is sent to the LTP after the Laser_emit pulse. The time between the Laser_emit and the calibration request is programmable in steps of 25nsec, setting a VME register of the SHAFT board. If the SLAMA doesn't send the Laser_emit signal the SHAFT doesn't send the calibration request to the LTP.

The CIS triggers are sent to a BGO input of the TTCvi. Two pulses are sent (one to open the charge injection and another one to close it). The time between the two pulses is programmable in steps of 25nsec, setting a VME register of the SHAFT board. The calibration request is sent to the LTP after the "close charge injection" trigger pulse. The time between the "close charge injection" pulse and the calibration request is programmable in steps of 25nsec, setting a VME register of the SHAFT board.

When BUSY is active, the calibration request for LASER and CIS are disabled. The trigger pulses are not blocked by the BUSY signal.

All the trigger pulses and the calibration request bits have a pulse width of 25 ns.

6. MEMORY MAP (RAM and internal registers)

The VME address bus of the SHAFT board has 24 bits. The address is divided in two parts: BASE + OFFSET.

$$\text{BASE} = \text{VME_ADDRESS}(23..16)$$

$$\text{OFFSET} = \text{VME_ADDRESS}(15..0)$$

The memory map (OFFSET part of the Address) is the following :

x0000 to x0FFF → RAM 4kBytes
x1000 to xFFFF → REGISTERS and NOT USED MEMORY POSITIONS

RAM

Operations: Read and write (**Data size 1 Byte**)

x0000 to x0FFF → RAM 4kBytes

REGISTERS:

There are 11 registers that can be set from the VME bus. The following table shows the VME address of these registers, the type, the DATA size and the possible values.

It is important to write and read to/from the VME bus using the same data size as it is specified for each register in the table, in order to read and write properly.

NAME	Address (Offset)	TYPE	Data size	VALUE
ENABLE_DISABLE12BITS_COUNTER	x1000	READ/ WRITE	1 Byte	XXXXXXXX1 → Enable XXXXXXXX0 → Disable
RESET	x1001	WRITE	1 Byte	any
ENABLE_DISABLE_TRIGGERS	x1002	READ/ WRITE	1 Byte	'1' → Enable '0' → Disable Bit0 → MB Bit1 → CIS Bit2 → LASER Others → not used
LASER_EMIT_SOURCE	x1003	READ/ WRITE	1 Byte	XXXXXXXX1 → NIM XXXXXXXX0 → LVDS
DELAY_TURN_MB_TRIGGER	x1004	READ/ WRITE	2 Bytes	Between x000 and xFFF (4 highest Bits are not used)
DELAY_TURN_CIS_TRIGGER	x1006	READ/ WRITE	2 Bytes	Between x000 and xFFF (4 highest Bits are not used)
DELAY_TURN_LASER_TRIGGER	x1008	READ/ WRITE	2 Bytes	Between x000 and xFFF (4 highest Bits are not used)
DELAY_CIS_OPEN_CLOSE_PULSES	x100A	READ/ WRITE	2 Byte	Between x000 and xFFF (4 highest Bits are not used)
DELAY_CIS_CLOSE_PULSE_CAL.REQ	x100C	READ/ WRITE	2 Bytes	Between x000 and xFFF (4 highest Bits are not used)
MB_TRIGGER_COUNTER	x100E	READ	1 Byte	Between x00 and xFF
DELAY_LASER_EMIT_CAL.REQ	x1010	READ/ WRITE	2 Bytes	Between x000 and xFFF (4 highest Bits are not used)

ENABLE_DISABLE12BITS_COUNTER: if the bit 0 is set to '1' the counter is enabled, and if it is set to '0' the counter is disabled. Other bits in the byte are not used.

RESET: writing to the VME offset address x1001 resets the 12 bit (TURN driven) counter and the state machine that generates the trigger pulses and the calibration request.

ENABLE_DISABLE_TRIGGERS: The triggers can also be disabled from the VME bus, setting the corresponding bit to '0'. By default the triggers are all enabled.

LASER_EMIT_SOURCE: The Laser_emit signal has two inputs at the SHAFT board, one is NIM and the other one is LVDS. If the bit 0 is set to '1' the NIM input is used, and if it is set to '0' the LVDS input is used. The other bits are not considered. By default the NIM input is used.

DELAY_TURN_MB_TRIGGER: The TURN signal arrives before the beginning of the GAP. The delay between the TURN and the MB calibration trigger has to be set in this register. Each count of this register corresponds to 1 BC period (25ns). Adjustable from 150 ns to 102.525 us.

DELAY_TURN_CIS_TRIGGER: The delay between the TURN and the CIS calibration triggers has to be set in this register. Each count of this register corresponds to 1 BC period (25ns). Adjustable from 150 ns to 102.525 us.

DELAY_TURN_LASER_TRIGGER: The delay between the TURN and the LASER calibration trigger has to be set in this register. Each count of this register corresponds to 1 BC period (25ns). Adjustable from 150 ns to 102.525 us.

DELAY_CIS_OPEN_CLOSE_PULSES: each count of this register corresponds to 1 BC period (25ns). Adjustable from 25 ns to 102.375 us.

DELAY_CIS_CLOSE_PULSE_CAL.REQ: Delay between the "close charge injection" trigger pulse and the calibration request. Each count of this register corresponds to 1 BC period (25ns). Adjustable from 25 ns to 102.375 us.

MB_TRIGGER_COUNTER: Shows the current number of MB triggers, and it is reseted each 256 counts.

DELAY_LASER_EMIT_CAL.REQ: Delay between the "Laser_emit" input pulse and the calibration request. Each count of this register corresponds to 1 BC period (25ns). Adjustable from 50 ns to 102.375 us.