

ATLAS Tile Calorimeter Electronics

Radiation Tolerance Qualification of the Integrator Readout Interface

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G. Blanchot

1. Introduction.

The Integrator Readout Interface, located in the drawer electronics of the Tile Calorimeter, must withstand radiation doses for 10 years of operation of the LHC. The board incorporates CMOS and bipolar devices and the radiation tolerance of the electronics parts used for production boards assembly must be insured according to the ATLAS Policy on Radiation Tolerant Electronics.

A pre-selection of components was performed in 1999 with ionising and neutron radiation tests, according to the radiation simulations (1998) and radiation tolerance policies available at that moment. Two CMOS devices failed in the ionising radiation test at 7 krad.

During year 2000, more simulations were carried out taking into account a more accurate geometry of the detector and board position. The resulting expected dose for the Integrator Readout Interface was reduced by about one order of magnitude. Because of this, the selected components are expected to pass the final radiation tolerance test.

In order to proceed with the full production, the final radiation test to qualify the parts for radiation tolerance was performed. Upon completion of the parts procurement, a production preserie was assembled and tested up to the RTC for total ionising dose, which is the most critical test. One of the two critical CMOS devices, the Altera PLD, was obtained from a controlled batch used for the 3in1 cards production. The second critical device, the CAN controller (SAE81C91), could not be certified to come from a single batch; however the entire lot was purchased from a single supplier.

The results of this latter test are described in this document and demonstrate that the Integrator Readout Interface boards will cope with the radiation levels expected in the LHC.

2. Radiation Tolerance Criteria.

There is one Integrator Readout Interface per superdrawer, plugged at the end of the first motherboard section. The board coordinates at the most sensitive location are:

$$Z = 210 \text{ cm}, R = 410 \text{ cm} \quad (\text{central barrel})$$

The expected total ionising dose and neutrons fluences for 10 years of LHC¹ operation are:

$$\begin{array}{ll} 1 \text{ MeV equivalent Neutrons:} & 3.7 \cdot 10^{10} \text{ n}^\circ / \text{cm}^2 \\ \text{Total Ionising Dose:} & 52 \text{ rad} \end{array}$$

The RTC can be computed from these expected doses, applying the required safety factors (the safety factors applied are given further below), and can be compared to the tests carried out in 1999:

	RTC (Production)	Tested Dose (1999)
TID	728 rad	50 krad, failure of Altera and CAN chips at 7krad.
NIEL	$7.5 \cdot 10^{11} \text{ n}^\circ / \text{cm}^2$	$10^{13} \text{ n}^\circ / \text{cm}^2$, no failure.

The final radiation test focused on the CMOS TID, because two failures were reported in 1999; despite these failures in 1999, there is still one order of magnitude of margin. For the NIEL test, the margin is greater than one order of magnitude, and because no failures were observed the test is not repeated.

The CMOS TID test procedure is shown on figure 1. The boards were monitored online for all the steps of the test.

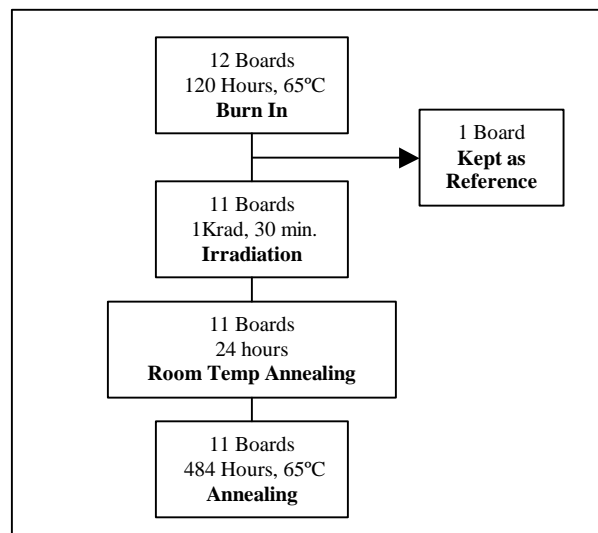


Figure 1: final test procedure for radiation tolerance certification of CMOS devices.

For the described procedure, the following safety factors apply to compute the radiation tolerance criterium:

- Simulation uncertainty safety factor: 3.5
- LDRE safety factor for CMOS devices is 1 (accelerated ageing applies).
- Uncontrolled components batches, safety factor is 4.
- $RTC-TID (CMOS) = 52 * 3.5 * 1 * 4 = 728 \text{ rad}$

3. Monitoring.

Two testbenches with a capacity for 6 boards were used. For each testbench, a monitoring program periodically checked the functionality of the boards through their CANBus port, writing a timestamped test report to an output logfile; in total, more than 500 MBytes of data were acquired. In order to monitor the ADC, a reference sinusoidal input signal was applied. In order to test the DAC that controls the global pedestal, a voltage sweep was generated through the DAC. The combination of the DAC sweep and of the input sine wave sampled by the ADC allowed to monitor online the conversion factors of the DAC and of the ADC. The monitoring program conforms to the block diagram described in figure 2.

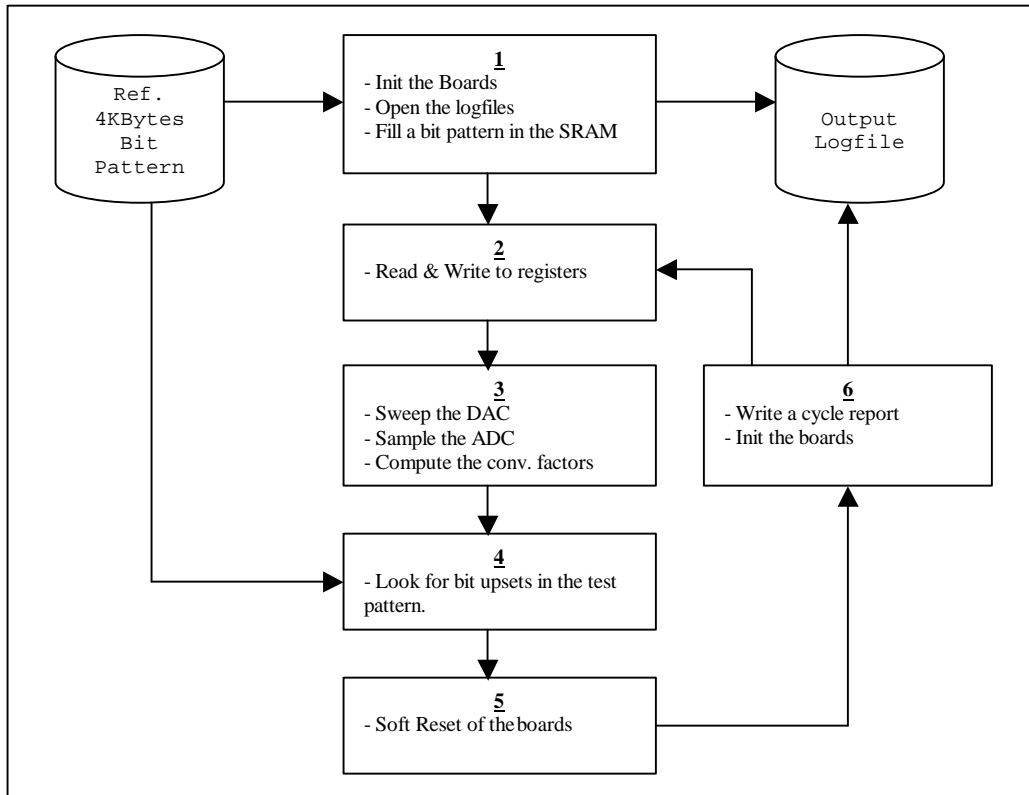


Figure 2: monitoring process, a complete cycle lasts about 1 minute.

4. Procedure results.

The test boards were burned in, irradiated up to 1krad, annealed at room temperature and at high temperature, following the described procedure. The irradiation was carried out at a dose rate of about 32 rad/min, with a calibrated Co -60 source used for radiotherapy at the Oncological Dept of the Hospital de Sant Pau (Barcelona). The test lasted for 32 minutes in total. In general and for all the procedure duration:

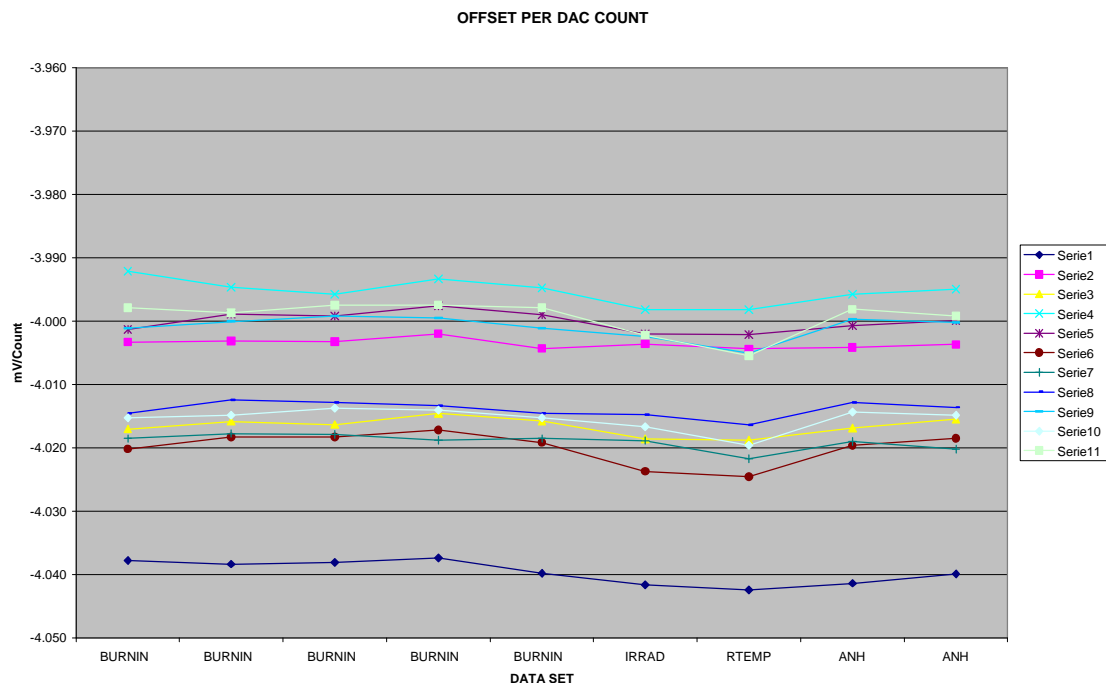
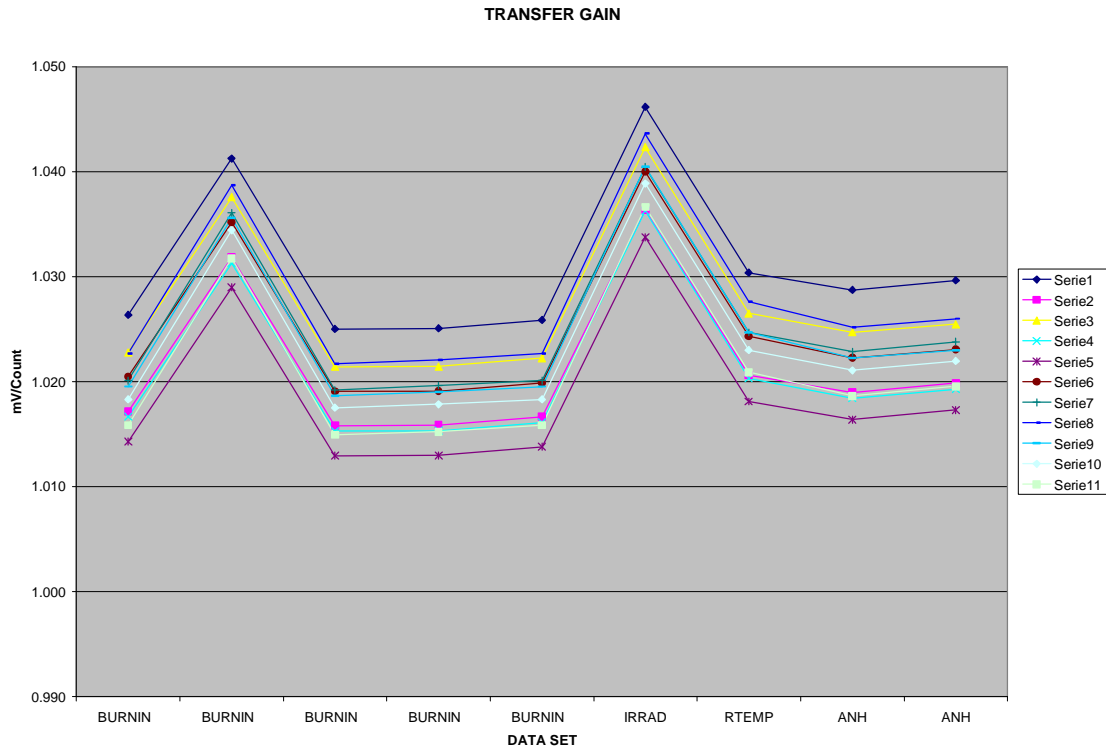
- The power consumption remained stable.
- No bit upsets were detected in the test bit pattern of the SRAM.
- The registers could be read and written.
- The DAC and ADC remained functional .
- All the boards remained functional up to the end of the procedure.

Nine data sets are represented for the 11 boards that were irradiated. The amounts of monitoring time of these data sets are:

BURN 1	BURN 2	BURN 3	BURN 4	BURN 5	IRRAD	R.TEMP	ANH 1	ANH 2
45 min.	15 hours	20 min.	72 hours	4 hours	30 min.	24 hours	300 h.	184 h.

The five burn in data sets were taken at different times over the total 120 hours of burn in. The two annealing data sets contain the total 484 hours of annealing.

In particular the average ADC transfer gain, i.e. the ADC counts per input millivolts, appears to be stable within 1% throughout the different monitoring steps for a given board. The dispersion is attributed to different power supply and temperature conditions. On the other hand, the DAC stability shown by the global offset per dac count appears stable at a level better than 0.25%. It must be note also that the two high temperature annealing data sets cover about 20 full days of data, however these results differ very little from the average values registered during the burn in periods: one could conclude from this that the irradiation step did not alter significantly the transfer gains of the ADC and of the DAC.



5. Summary and conclusions.

The CMOS TID test was carried out in order to insure the radiation tolerance of the CMOS devices, and in particular of the Altera chip (EPM7064STC44 -10) and of the Siemens CAN controller (SAE81C91) that failed at 7krad in 1999. The Altera chip was obtained from the controlled batch used for the 3in1 cards production, for which the radiation tolerance is greater than 10krad. The CAN chip, and the rest of components, come from an uncontrolled batch: for this reason the safety factor for uncontrolled batches has been applied.

To insure the reliability of the test boards, a burn in period of 120 hours was applied in order to reject any unreliable board before proceeding with the irradiation test. All boards passed the burn in successfully, and consequently the probability of board failures that are not related to the irradiation test, is reduced.

In order to be as close as possible to the low dose rate environment in ATLAS, the irradiation was carried out at the lowest dose rate that the facility could provide (32 rad/min), and in addition to this an accelerated ageing of 20 days at 65°C has been carried out.

It must be noted that from the preliminary burn in until the end of the accelerated ageing, no variation has been observed in the power consumption; in 1999, the power consumption increased significantly before the failure. This fact indicates that the boards are still in a safe operation range after the total ionising dose has been applied.

No failures have been reported at all during any of the test steps (burn in, irradiation, room temperature annealing, high temperature annealing). During the annealing period, no significant drift of the ADC and DAC transfer gains have been observed, which indicates that the internal voltages references are not sensitive to low dose rate effects for the required ionising dose.

In view of these results, the CMOS components of the Integrator ADC boards are qualified for operation in low dose rate environment for 10 years of LHC operation. In view of the test carried out in 1999, the rest of components used in the Integrator ADC board are qualified for operation in ionising dose and neutrons fluence radioactive environments for more than 10 years of LHC operation.

¹ ATLAS Policy on Radiation Tolerant Electronics (Appendix 1): ATLAS Radiation Tolerance Criteria for Electronics Components, Sub-part of ATC-TE-QA-0001, revision 2, 21 July 2000.