

ATLAS Tile Calorimeter Electronics

NIEL Tolerance Qualification of the Integrator Readout Interface

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1. Introduction.

The Integrator Readout Interface, located in the drawer electronics of the Tile Calorimeter, must withstand radiation doses for 10 years of operation of the LHC. The board incorporates CMOS and bipolar devices and the radiation tolerance of the electronics parts used for production boards assembly must be insured according to the ATLAS Policy on Radiation Tolerant Electronics.

A pre-selection of components was performed in 1999 with ionising and neutron radiation tests, according to the radiation simulations (1998) and radiation tolerance policies available at that moment. During the year 2000, more simulations were carried out taking into account a more accurate geometry of the detector and board position and the final CERN policy for radiation tolerant electronics in ATLAS was defined. A final TID tolerance test was successfully carried out (during year 2000) on 11 production boards that showed no failures up to a radiation tolerance criterium (RTC) of 10 Gy.

The pre-selection NIEL test carried out at the PROSPERO reactor in 1999 on two prototypes showed that a voltage reference suddenly drifted down by about 20% at a fluence of $5 \cdot 10^{12}$ n^o/cm². During this test, boards were monitored online showing a good behaviour of the voltage reference up to this fluence. More recently (2003), 10 of the production boards exposed to 10 Gy for TID qualification in 1999 were exposed to a neutrons fluence of $1 \cdot 10^{12}$ n^o/cm² in Portugal. During this final NIEL qualification test, boards were unpowered and could not be monitored online. However, after the test, the voltage reference appeared to have drifted down on all cards by about 15%.

The results of this latter test are described in this document and demonstrate that the Integrator Readout Interface boards will conform with the required neutron fluence RTC and evaluates the impact of the observed drift on the experiment.

2. Radiation Tolerance Criteria.

There is one Integrator Readout Interface per superdrawer, plugged at the end of the first motherboard section. The board coordinates at the most sensitive location are:

$$Z = 210 \text{ cm}, R = 410 \text{ cm} \quad (\text{central barrel})$$

The expected total neutrons fluence for 10 years of LHC¹ operation is:

$$\text{SRL:} \quad 3.7 \cdot 10^{10} \text{ n}^{\circ} / \text{cm}^2 \quad [1 \text{ MeV equivalent Neutrons}]$$

The RTC can be computed from these expected doses, applying the required safety factors:

$$\text{RTC:} \quad 7.5 \cdot 10^{11} \text{ n}^{\circ} / \text{cm}^2 \quad [1 \text{ MeV equivalent Neutrons}]$$

3. Past results.

Two samples were previously tested up to a fluence of $1 \times 10^{13} \text{ n}^\circ/\text{cm}^2$ at PROSPERO(1999), showing a drift of the ADC (MAX190BCWG from MAXIM) internal voltage reference. This voltage reference was monitored online during this preliminar test and showed that the drift started at a fluence threshold of $5 \times 10^{12} \text{ n}^\circ/\text{cm}^2$, then the voltage reference drifted down quite fast and remained stable afterwards (Figure 1). The same effect was previously recorded during a TID test in 1998 at CIEMAT (Madrid) up to a dose of 500Gy at a dose rate of 150 Gy/hour (Figure 2). In this last case, the boards were monitored online up to a dose of 70 Gy without any drift in the voltage reference. The final TID qualification test up to 10 Gy showed no drift.

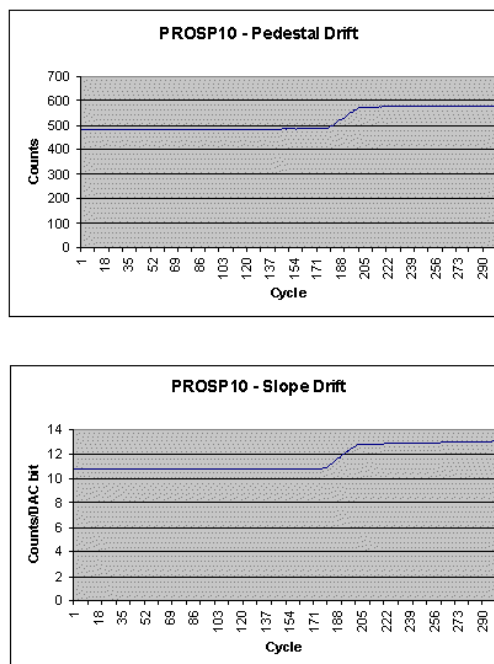


Figure 1: voltage reference drift observed at Prospero at a fluence of $5 \times 10^{12} \text{ n}^\circ/\text{cm}^2$.

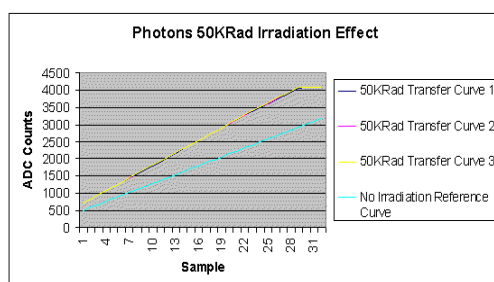


Figure 2: voltage reference drift observed at CIEMAT for a total dose of 500Gy.

It can be concluded from these past tests that the ADC internal voltage reference is sensitive to photons at a dose greater than 70 Gy and to neutrons at a fluence of $5 \times 10^{12} \text{ n}^\circ/\text{cm}^2$. These effects occurred at levels beyond the required RTCs for this device.

4. NIEL Tolerance Qualification Test.

The 10 boards exposed to a total ionising dose of 10 Gy for TID qualification in the year 2000 were exposed again in 2003 to a neutron fluence of $1 \cdot 10^{12}$ n^o/cm² in order to fully qualify them for its use in ATLAS. An additional board was kept as reference. The exposure took place at the reactor of the Instituto Tecnológico Nuclear (ITN) at Socavem, Portugal. The new policy for radiation tolerant electronics did not require the boards to be powered, hence they were not monitored online. The 11 boards were extensively tested on their QC testbench before and after exposure. Concurrently with the neutron fluence, the boards were exposed to up to 66 Gy of residual photons. Because the boards were unpowered, no effects were expected from the latter.

The 11 boards passed the quality control process used during mass production, mainly focused on the functionality of the boards:

- Initialization.
- In-system reprogrammability test of both memories through CANBus.
- Check of programmed serial number.
- Check of internal parameters (read/write into registers through CANbus).
- Check with an oscilloscope of the onboard DAC that controls a global pedestal.
- Check with an oscilloscope of the 3in1 control serial interface.
- Check of the ADC for different values of the DAC.
- Measurement of a sine wave at a sampling rate of 100 Hz.
- Measurement of the ADC voltage reference (direct measurement with a tester).

This quality control test covers all the functionalities of the cards, including the in-system reprogrammability, the serial interface, and the analogue to digital conversion path. For this last item, the voltage reference of the ADC is measured by means of direct measurement on the MAX190 Vref pin. The precision of the DAC is measured by means of direct measurement on the AD557 output pin.

The MAX190BCWG voltage reference nominal value is 4.096 Volts with a resolution of 12 bits (1mV/count). The AD557 used for pedestal control has a nominal range of 2.56V with a resolution of 8 bits (10mV/count).

5. Test results.

All 10 irradiated cards maintained their functionality after irradiation, including in system programmability, CANBus communication, parameters control and analogue conversion path. The MAX190BCWG chip remained functional, however a drift in its voltage reference was observed and confirmed by means of direct measurement on the Vref pin. The DAC and ADC conversion factors are summarized in Table 1.

It can be observed from the summary table (Table 1) that the DAC conversion factor didn't drift. However the voltage reference of the cards exposed to neutrons drifted down by about 15% in average, while the card kept as reference (not exposed to neutrons) did not drift.

This result differs significantly from that obtained with the PROSPERO test. There, a drift was also observed but at a fluence of $5 \cdot 10^{12}$ n^o/cm². In this new test, the neutron fluence was contaminated with photons and cards were then exposed to residual photons up to 66 Gy. Despite the fact that cards were not powered, the voltage reference drift can either be attributed to the neutron fluence ($1 \cdot 10^{12}$ n^o/cm²) or to the residual photons (66 Gy).

Serial Number	Before NIEL Test			After NIEL Test				
	DAC [mV/Count]	ADC [mV/Count]	ADC Vref [mV]	DAC [mV/Count]	ADC [mV/Count]	ADC Drift [%]	ADC Vref [mV]	Vref Drift [%]
PS2001 (Ref.)	10.0	0.947	4.09	10.0	0.946	0.1	4.09	0.0
PS2002	10.0	0.948	4.09	10.0	0.797	15.9	3.43	16.1
PS2003	10.0	0.951	4.09	10.0	0.868	8.7	3.78	7.6
PS2004	10.0	0.948	4.09	10.0	0.799	15.7	3.45	15.6
PS2005	10.0	0.952	4.09	10.0	0.800	16.0	3.47	15.2
PS2006	10.0	0.946	4.09	10.0	0.797	15.8	3.45	15.6
PS2007	10.0	0.948	4.09	10.0	0.792	16.5	3.44	15.9
PS2008	10.0	0.941	4.09	10.0	0.782	16.9	3.53	13.7
PS2009	10.0	0.945	4.09	10.0	0.795	15.9	3.52	13.9
PS2010	10.0	0.948	4.09	10.0	0.792	16.5	3.42	16.4
PS2011	10.0	0.949	4.09	10.0	0.827	12.9	3.60	12.0

Table 1: NIEL Test Summary Table. The card PS2001 wasn't exposed to neutrons and is used as reference card.

Because the DAC output remained stable for both photons and neutrons tests, it is possible to calibrate the ADC voltage reference by applying a reference pedestal slope that covers all the DAC output range, as is done during the quality control process. The slope measured in counts by the ADC is directly proportional to its internal voltage reference, and a cross calibration can then be performed in this way with good accuracy. Hence, this drift will have a very limited impact on the minimum bias monitoring system and on the cesium calibration system if periodical cross calibrations are done as mentioned.

On the other hand, past result show that the drift occurs at a given neutrons fluence threshold close to the RTC. It can be expected that for many years of operation of the LHC, no drift will be observed. If the ADC integrator cards will be exposed to a fluence smaller than the RTC for the 10 years of operation, the drift threshold may never be reached.

If such such a drift occurs, it can be corrected by periodical cross calibrations of the ADC voltage reference using the onboard DAC output.

6. Summary and conclusions.

Ten integrator ADC boards have been exposed to a neutrons fluence of $5 \cdot 10^{12} \text{ n}^\circ/\text{cm}^2$ with 66 Gy residual photons in Portugal. An additional board was used as reference and wasn't irradiated. The boards passed successfully all the functional tests of the quality control procedure before and after irradiation.

One component appears to be sensitive to either neutrons and/or photons. Past tests already revealed the sensitivity of this component for both neutrons and photons. This component is an analogue to digital converter from MAXIM (MAX190CWG), and the sensitive element is its internal voltage reference that could be measured directly on one of its pins. The digital interface of this chip wasn't affected by the neutrons fluence. After irradiation, an average drift of 15% was observed. Because the neutron fluence of the ITN facility was contaminated with photons contributing a dose greater than the TID radiation tolerance criterium, it is not possible to conclude which beam component has induced this drift.

The past tests showed the neutron-induced drift occurs at a fluence value close to the RTC. Because of this, for most of the time of operation of ATLAS, no drift is expected. However, if it ever occurs, the ADC internal reference can be cross-calibrated by using the onboard DAC which was proven to be insensitive to

neutrons and photons up to the respectively required RTCs. The minimum bias monitoring system and the cesium calibration system, which use the tested device, will require periodical cross calibrations of the internal voltage reference as described.

¹ ATLAS Policy on Radiation Tolerant Electronics (Appendix 1): ATLAS Radiation Tolerance Criteria for Electronics Components, Sub-part of ATC-TE-QA-0001, revision 2, 21 July 2000.